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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,685	10/23/2003	Chi-Yang Lin	3304.2.96	6603
21552	7590	09/09/2005	EXAMINER	
MADSON & METCALF GATEWAY TOWER WEST SUITE 900 15 WEST SOUTH TEMPLE SALT LAKE CITY, UT 84101			SINGH, DALIP K	
			ART UNIT	PAPER NUMBER
			2671	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/691,685

Applicant(s)

LIN ET AL.

Examiner

Dalip K. Singh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S.

2001/0040581 A1 to Reddy in view of U.S. Patent No. 6,006,248 to Nagae.

- a. Regarding claim 1, Reddy **discloses** integrated graphics display memory elements (IGDM) 108 including a graphics accelerator 110 connected between a data output bus 104 and CPU 102 [page 2, paragraph 23-26]. However, Reddy **is silent about** detecting a utilization rate of said central processing unit and allocating said graphics data to either said central processing unit or said graphics processor according to said utilization rate of said central processing unit. Nagae **discloses** detecting a utilization rate of central processing unit (...threshold of the CPU usage rate...which is defined as a difference of the CPU usage rate between the main computer 1 and the other computer 13...the computer specifying means 8 is so constructed that...decided to move the job application to the other computer...col. 15, lines 25-45) and allocating data to either central processing unit or graphics processor. Nagae is not specifically teaching a central processor and a graphics unit but a main computer and other computer; which is similar to the claim limitation where data is processed in either central processing unit or graphics processor based on the utilization rate of said central processing unit. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Reddy with the feature "detecting

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a utilization rate of central or main processor and allocating data to central or main processor or other computer according to utilization rate of the central or main processor” as taught by Nagae **because** it allows to level a load among computers and thereby allow each computer to efficiently execute a job application (col. 1, lines 55-65).

b. Regarding claim 2, Reddy **discloses** wherein said graphics data are vertex data generated by an application program (...a central processing unit that generates both display data and graphics commands for processing the display data...page 1, paragraph 15).

c. Regarding claim 3, Reddy as modified by Nagae **discloses** wherein said step of detecting said utilization rate of said central processing unit is performed by periodically sampling command flows of said central processing unit (...the load information table 7 of the first embodiment stores the CPU usage rate of each computer and an index indicative of a CPU performance of each computer (CPU performance value) therein...The CPU performance value may be the number of instruction execution per unit time (such as a MIPS (Million Instruction Per Second)) or a relative performance value which is compared to the performance value of a particular computer as a certain criterion and indicates how degree of a CPU processing performance each computer has. That is, as long as each computer has the same index, any performance value as to the CPU can be used...col. 17, lines 65-67; col. 18, lines 35-45).

d. Regarding claim 4, Reddy **does not disclose** allocating said graphics data to said transformation/lighting engine of said graphics processor when said utilization rate of said central processing unit is equal to or greater than a threshold value; and allocating said graphics data to said central processing unit when said utilization rate of said central processing unit is less than said threshold value. Nagae **discloses** allocating graphics data **to graphics processor** when said utilization rate of central

processing unit is equal to or greater than a threshold value (...Referring to FIGS. 1 and 10, the computer specifying means 8 decides whether or not the CPU usage rate of the main computer 1 exceeds the threshold of the CPU load (step 1001). When the CPU usage rate exceeds the threshold, it is decided whether or not the CPU usage rate of the other computer 13 is lower than that of the main computer 1 (step 1002). When the CPU usage rate is lower, the CPU usage rate difference between the main computer 1 and the other computer 13 is obtained (step 1003). **It is decided whether or not the difference is equal to or more than a value of the CPU load allowance (step 1004). When the difference is equal to or more than the value of the CPU load allowance,** the identification information of the other computer 13 and the information as to the job application distribution are stored in the computer information table 10 so as to **move the job application** prior to scheduling **to the other computer 13** having the allowance of the CPU (step 1005)...col. 16, lines 6-26); and allocating said graphics data to said central processing unit when said utilization rate of said central processing unit is less than said threshold value (...When the **difference is less than the value of the CPU load allowance,** the identification information of the main computer 1 and the information as to the job application distribution are stored in the computer information table 10 so as to execute all the job application in the main computer 1 (step 1006)...col. 16, lines 26-31). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Reddy with the feature "allocation of graphics to the graphics processor (other computer 13) when utilization rate of central processing unit is equal to or greater than a threshold value; and allocating central processing unit when utilization rate of CPU is less than the said threshold value" as taught by Nagae **because** the load is leveled

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among the central processing unit and graphics processor with job application being executed efficiently (col. 26, lines 47-50).

e. Regarding claim 5, Reddy **discloses** wherein said digital data processing system is a computer system (...a shared memory graphics accelerator system 100 that includes a central processing unit (CPU)...page 2, paragraph 23).

f. Regarding claim 6, it is similar in scope to claim 1 above and is rejected under the same rationale.

g. Regarding claim 7, it is similar in scope to claim 2 above and is rejected under the same rationale.

h. Regarding claim 8, Reddy as modified by Nagae **discloses** when although the job application has the load which is not very so high if the load is averaged, it is decided to move the job application to the other computer. However, Nagae allows the inappropriate job application distribution to be prevented, which is the limitation where the first threshold and second threshold value is identical, a sort of debounce mechanism where jobs are not moved back and forth between a central processing unit and a graphics processor (col. 26, lines 15-24).

i. Regarding claims 9 and 12, they are similar in scope to claim 3 above and is rejected under the same rationale.

j. Regarding claim 10, it is similar in scope to claim 5 above and is rejected under the same rationale.

k. Regarding claim 11, it is similar in scope to claim 1 above and is rejected under the same rationale.

l. Regarding claim 13, it is similar in scope to claim 4 above and is rejected under the same rationale.

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- m. Regarding claim 14, Reddy **discloses** wherein said path selection unit is incorporated in a chip (...fig. 2 shows a shared memory graphics accelerator system 100 that includes a central processing unit...via a control bus 106 to a single integrated graphics display memory (IGDM) 108...page 2, paragraph 23)
- n. Regarding claims 15 and 16, Reddy as modified by Nagae **discloses** main computer 1 and the other computer 13 are provided with recording media 14 which records the program for the execution of the processing, thereby suggesting hardware as well as firmware implementation, as it could be written as a embedded program in the recording media 14 (col. 26, lines 25-45).
- o. Regarding claim 17, it is similar in scope to claim 2 above and is rejected under the same rationale.

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Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**.


The examiner can normally be reached on Mon-Friday (10:30AM-6:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh
Examiner, Art Unit 2671

dks
September 5, 2005


ULKA J. CHAUHAN
PRIMARY EXAMINER